TIE-50206 Logic Synthesis, Final Exam / Midterm Exam 2
Thu 4.3.2016

Name: _____

Student no. _____

Final Exam: Answer every question

2nd Midterm Exam: Answer only questions 4-6

Made by: Arto Perttula

Students can use **any calculator** or dictionary.

Moreover, each student can have 1 A4 sheet of **own notes**. There are no restrictions about their style and they are not collected.

Students can do anything they wish with the exam paper.

In addition to text, use figures, tables, equations, and examples in your answers.

In logic diagrams, you can use basic gates (AND, OR…), flip-flops, multiplexers, and common arithmetic components (adder, subtractor, multiplier, comparator…).

Mark the name of every signal and indicate their width clearly.

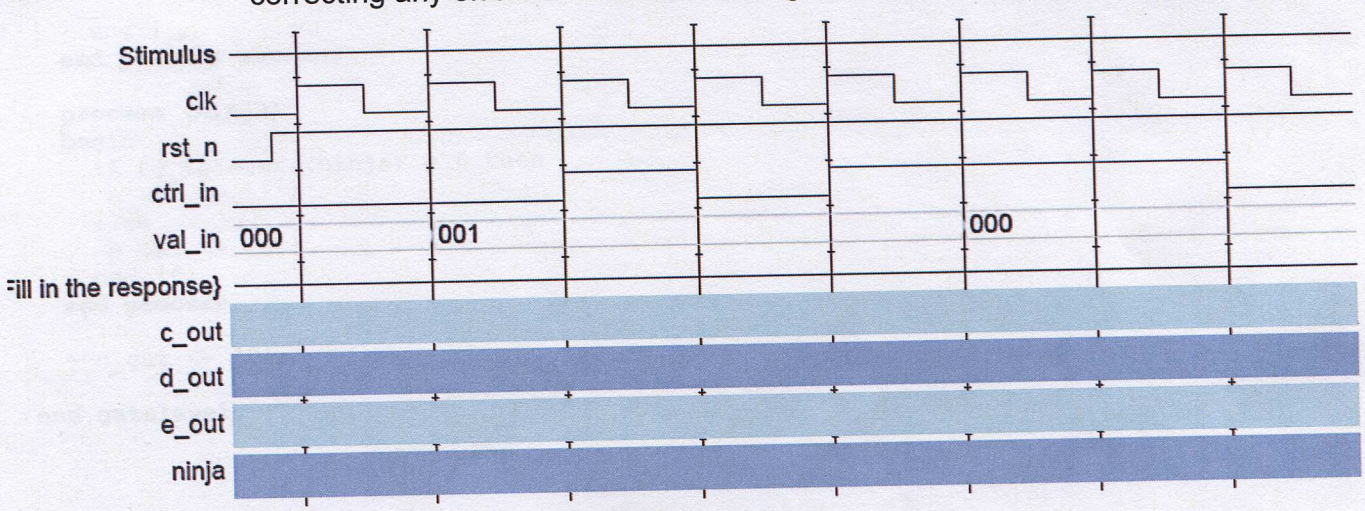
Preferably write your answers in numerical order (1a, 1b, … 6).

Please answer in Finnish if possible, eli vastaa suomeksi jos vain osaat.

1. Answer and explain (4p)
   a) Terms: signal's event and delta delay (2p)
   b) What is the difference between architecture types RTL and structural (2p)

2. State machines(4p)
   a) Give an example how Mealy state machine differs from Moore state machine (2p)
   b) What are the basic styles to implement state machines with VHDL? What differences there are in practice between them? (2p)

3. Analyze the code in the following page. The clock period is 10 ns. (7p)
   a) What errors or suspicious structures there are in the code? (There is no syntax errors) (3p)
   b) Fill in the timing diagram below directly according the code, i.e., without correcting any errors. Present the timing as simulator interprets it. (4p)



Name: _____

Student no. _____

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity tentti is
  generic (
    data_width_g : integer := 3);
  port (
    clk     : in  std_logic;
    rst_n   : in  std_logic;
    ctrl_in : in  std_logic;
    val_in  : in  std_logic_vector (data_width_g-1 downto 0);
    c_out   : out std_logic;
    d_out   : out std_logic_vector (data_width_g-1 downto 0);
    e_out   : out std_logic_vector (data_width_g-1 downto 0)
    );
end tentti;

architecture gatelevel of tentti is

  signal ninja : unsigned ( data_width_g-1 downto 0);


begin

  tenho: process (ctrl_in, ninja, val_in)
  begin
    if ctrl_in = '1' then
     e_out <= not val_in after 4 ns;
    else
     e_out <= val_in after 4 ns;
    end if;
  end process tenho;

  sauren : process (clk, rst_n, ninja)
    variable tmp_v : unsigned (3-1 downto 0);
  begin
    if rst_n = '0' then
      ninja <= (others => '0');

    elsif clk'event and clk = '1' then
      tmp_v := ninja+1;
      d_out <= std_logic_vector(tmp_v);
      ninja <= ninja +2;

    end if;
  end process sauren;

  process (ninja)
  begin
    if to_integer (ninja) = 6 then
     c_out <= '1';
    else
     c_out <= '0';
    end if;
  end process;

  --c_out <= '0';

end gatelevel;
```

Name: _____
Student no. _____

4. Analyze the VHDL code on the previous page. Show the resulting logic diagram after RTL syntehsis.Use dashed line to show separate synthesized logic of each process. Show every port, signal and variable. Don't make too small or ugly diagram, but clear and elegant. (6p)

5. Clocking (4p)
   a) What means the term *clock domain*? Draw a figure where it exists. What is the result of it or is there any results? (2p)
   b) Why would it be desirable to use many clock signals in the same chip? (2p)

6. Analyze the test circuit below (5p)
   a) How the metastability is detected in basic RTL-simulation? (2p)
   b) How the test circuit works? (Hint: in addition to text, draw a small timing diagram where something interesting happens) (3p)

Figure 4. Test Circuit Structure for Metastability Characterization

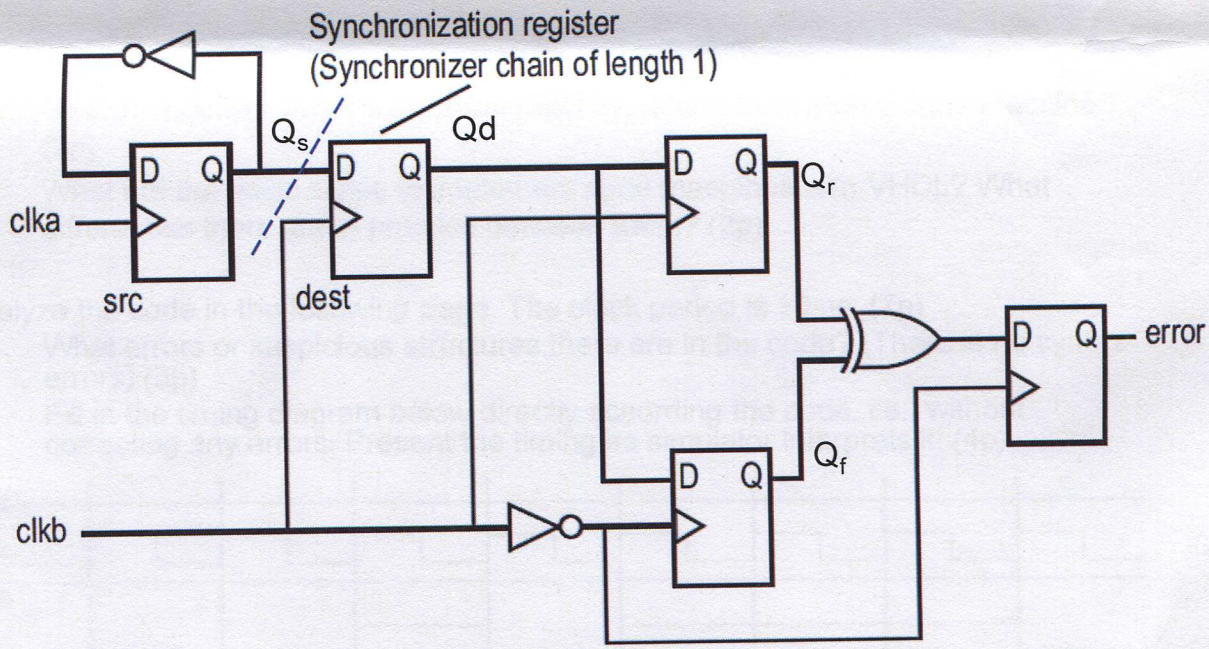


Figure t5. Test Circuit